ATLAS TRT Barrel Electronics Cooling: Duke mockup measurements and FEA calculations

W. Ebenstein, J. Fowler, S. Oh, V. Vassilakopoulos, and C. Wang

Department of Physics, Duke University
Durham, North Carolina 27708

This report summarizes measurements and calculations using the most recently proposed cooling scheme, shown in Fig. 1. Heat generated by the ASDBLR and DTMROC stamp boards is conducted to an aluminum plate sandwiched between the upper and lower stamp boards (hereafter referred to as the 'middle cooling plate'). The heat is then carried up through a vertical aluminum post, and finally to a large aluminum plate above all of the upper stamp boards (the 'upper cooling plate'), to which cooling tubes are attached.

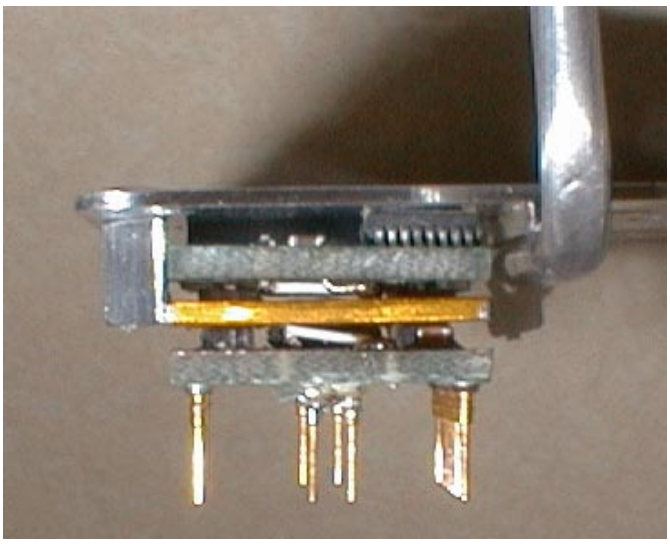


Fig. 1. A portion of the cooling mockup, as described in the text. The color of the middle cooling plate is due to a covering of Kapton tape. The full mockup has 21 such stacks.

Details of the mockup construction

The mockup is basically the same one used for the past several years for electronics cooling studies, consisting of the stamp board sets and roof boards supplied by Lund (see http://www.quark.lu.se/~bjorn/trt/temp_module.html) plugged into a Type 1 tension plate of 1.5 mm thickness. For the present studies we modified the stamp boards to more closely simulate the effects of having the ASDBLR's on the top of the lower stamp board and the DTMROC's on the bottom of the upper stamp board. This consisted of mounting resistors on the stamp boards (Fig. 2). For the present studies the resistors were chosen to produce 40 mW/channel from the ASDBLR board and 60 mW/channel from the DTMROC board at a nominal 5 VDC.

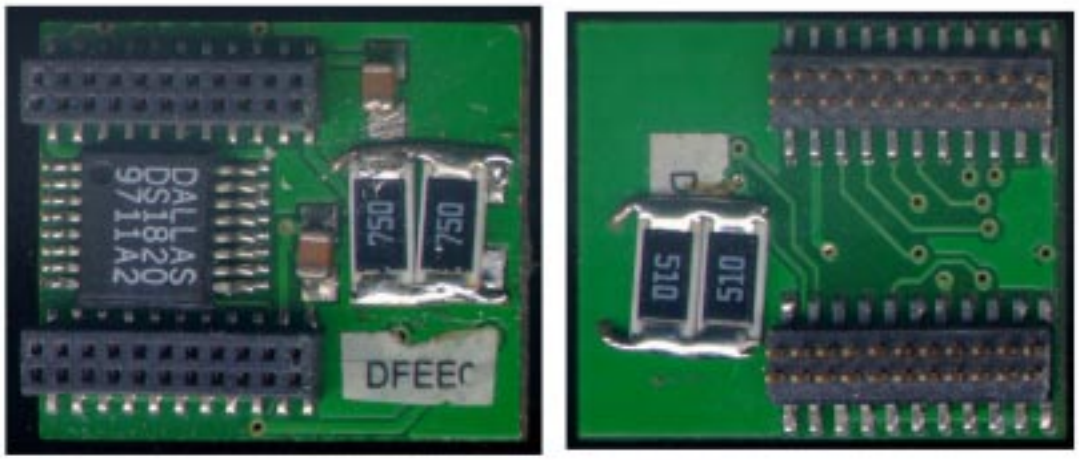


Fig. 2. The modified stamp boards. The left is the top of the ASDBLR board and the right is the bottom of the DTMROC board.

For all of the present measurements, heat sink compound (zinc oxide in silicone grease, κ ~ 0.8 W/m-K) was used to fill the volume between the middle cooling plate and each of the two stamp boards (κ ~ 0.23 W/m-K used for G-10/FR4). Results were also obtained with and without grease filling the space between the DTMROC board and the upper cooling plate (Fig. 3). These will be referred to as scheme A and B, respectively.

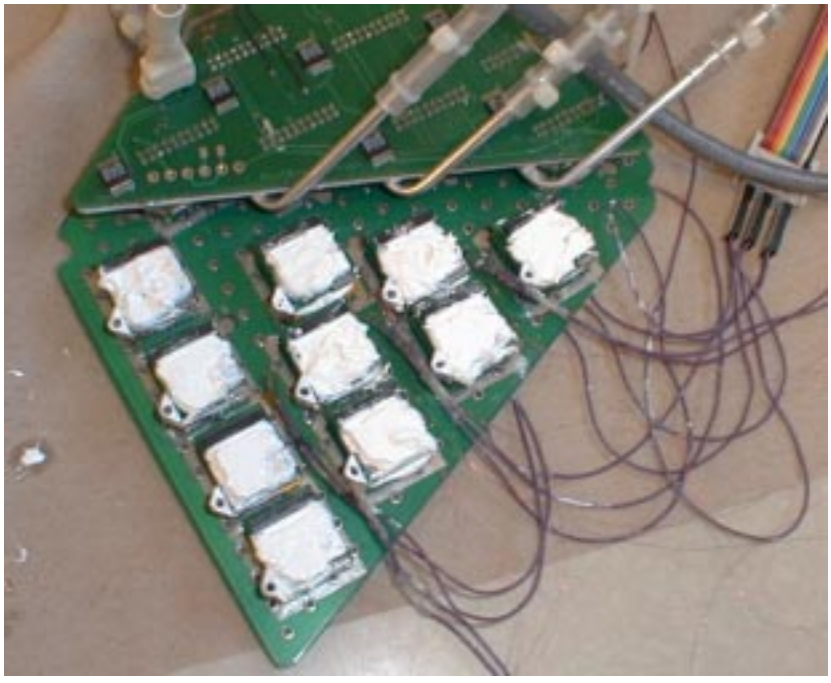


Fig. 3. Complete mockup with one roof board and upper cooling plate removed, showing grease applied to tops of DTMROC boards. Three thermistors can be seen attached to the tension plate and one attached to the vertical post of a middle cooling plate.

Water was the cooling fluid, flowing at 0.4 liters/min at an inlet temperature of 15°. The cooling tubes were attached to machined saddles on the underside of the upper cooling

plate with silver epoxy (κ ~ 3 W/m-K). Type 1100 aluminum (κ ~ 220 W/m-K) was used for the middle and upper cooling plates, with the masses being 0.56 g each for the middle plates (includes vertical post) and 32.5 g total for the two upper plates, not including tubing. The total aluminum in the mockup is then 44.3 g, which divided by the area of a type 1 tension plate (160 cm^2) is an effective thickness of 1.0 mm. For reference, in the mockup the aluminum is 73% upper plate, 20% middle plate, and 7% vertical post.

Results of measurements and calculations

Average temperatures (°C) obtained with {40 + 60} mW / channel are shown in Table 1. Note that the entries labeled "chip surface" represent the maximum temperature at which the electronics chip is in contact with its stamp board.

Table 1. Mockup results and ANSYS calculations for baseline dimensions.

Location	(A) With grease above DTMROC		(B) Without grease		(C) Adding DTMROC insulator	
	Mockup	ANSYS	Mockup	ANSYS	Mockup	ANSYS
Tension plate	35	37	40	42	-	30
ASDBLR (PCB)	35	37	39	42	-	30
ASDBLR (chip surface)		37		43		30
DTMROC (PCB)	*	29	*	43	-	42
DTMROC (chip surface)		37		44		60
Grease above middle plate	36	36	42	42	-	-
Upper cooling plate	22	21	23	23	-	19

* The sensors on the tops of the DTMROC boards do not provide useful data in this case due to close proximity to (or contact with) the upper cooling plate.

Comparing schemes A and B, it is clear that the presence of a good thermal path (the grease) from the top of the DTMROC board to the upper cooling plate is an important factor. This means that the electronics connector on top of the stack should use as little area as possible and the spacing between the top of the stack and the upper cooling plate should be minimized (this distance is 2 mm in our mockup due to components mounted on the upper side of the DTMROC board). Next compare scheme A with C, which restores the grease above the DTMROC board but removes it between the middle cooling plate and the DTMROC, instead filling this space with a thermal insulator. This could not be tested with the mockup, but it is expected that this scheme will achieve the lowest tension plate temperatures by channeling the DTMROC heat mostly upwards, albeit through the poor thermal conductor of the G-10/FR4 board on which the DTMROC is mounted. It is clear that this is indeed the bottleneck, so the upper stamp board material should be kept as thin as possible, and PCB material with maximum thermal conductivity should be used.

Details of the FEA calculations

We have used ANSYS software to model a single set of stamp boards with middle and upper cooling plates. The goal of this is to enable us to understand the heat flow / bottlenecks in the mockup, and to let us vary material properties and thicknesses over a broader range than we could do practically by building mockups. The elements included in the FEA model are shown in Fig. 4, which illustrates the three main variations we examined.

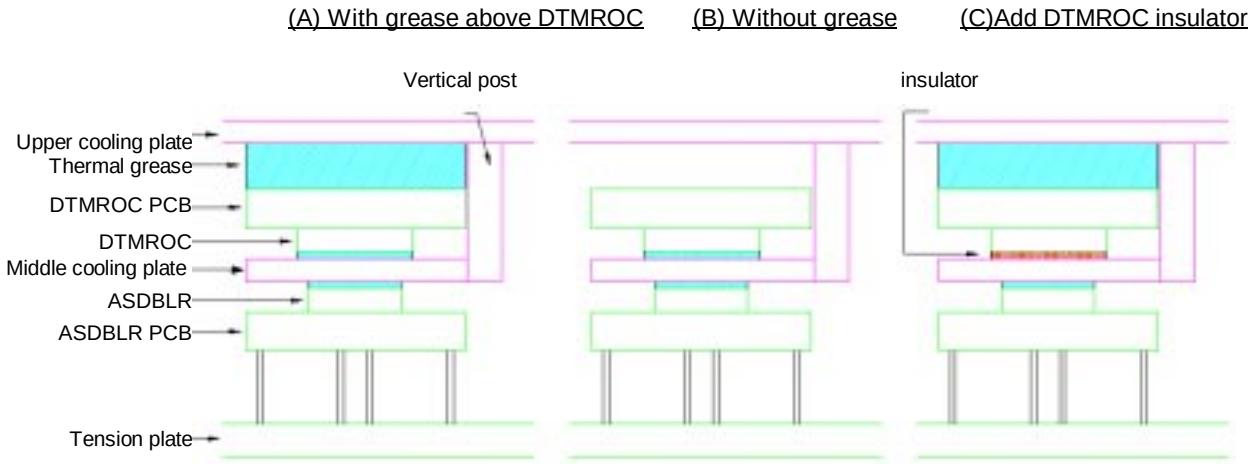


Fig. 4. Schematic illustration of cooling schemes A, B, and C, as described in the text. The vertical scale has been expanded by 2x for clarity.

The graphical output of one run of scheme A is shown in Fig. 5. In order to report temperatures in Table 1 that can be compared with those from the mockup, we used (min + max)/2 for average temperatures from the ANSYS output. Our 'baseline' configuration for the calculations had a total aluminum mass of 48.3 g, which yields an effective thickness of 1.1 mm, and it is this configuration that is shown in Table 1. As

the table shows, Scheme C minimizes the tension plate temperature at the cost of higher DTMROC temperature.

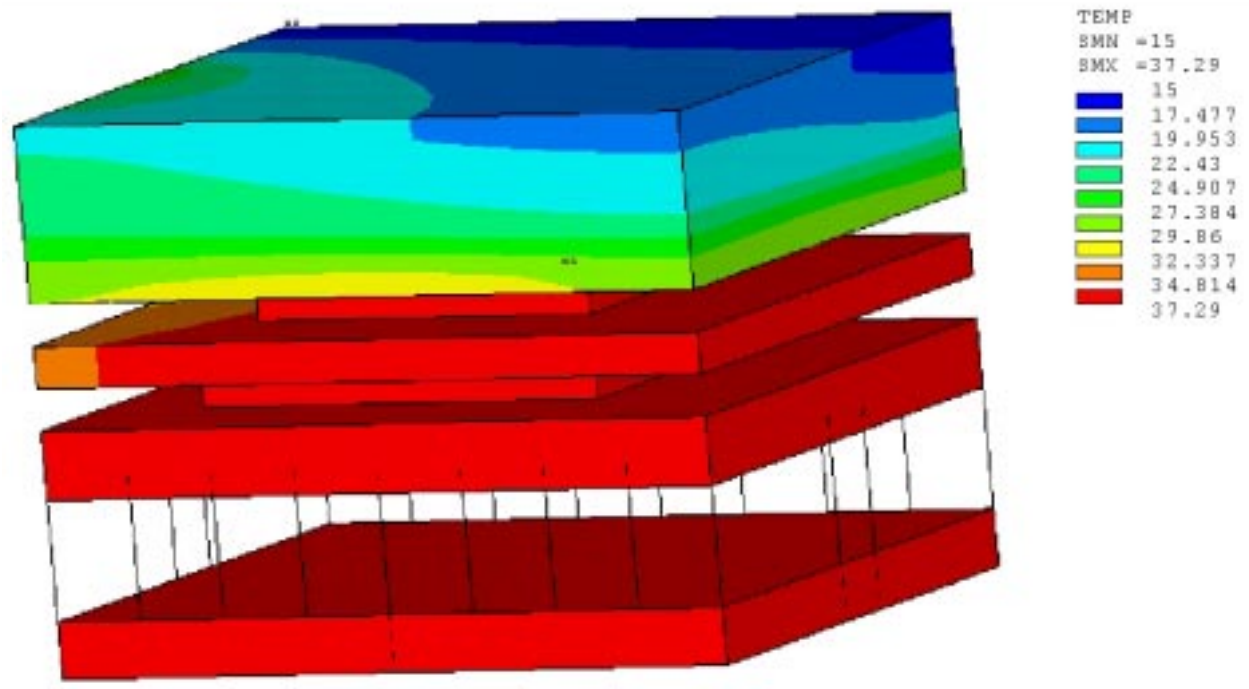


Fig. 5. Sample ANSYS output for scheme A. The cooling tube (not shown) is in contact along the entire top back edge, and the vertical cooling post (not visible) is at the left edge.

Optimization (ANSYS calculations)

For these calculations we chose conditions that incorporate possible improvements in the baseline configuration. These changes are as follows: thickness of DTMROC stamp board decreased from 1.7 mm to 1.0 mm; distance from top of DTMROC stamp board to upper cooling plate decreased from 2 mm to 1 mm. The aluminum mass is not changed. Note that this does not represent a numerical global optimization of all adjustable parameters, which we may do at a later date. These results are shown in Table 2, with the previous results for scheme C repeated for comparison. These show a clear improvement in the DTMROC temperature, and more closely represent a future flex circuit design. Another change, not shown in the table, involves changing the area of the DTMROC chip itself. In all of our calculations, this area was 90 mm^2, but if it is changed to 150 mm^2, better spreading out the heat load to the DTMROC board, the DTMROC temperature decreases ~ 4° from the values shown in Table 2.

Additionally, we have investigated the effect of changing the amount of aluminum. These results will not be presented here, but they indicate that there is adequate material in the baseline configuration, and an increase of ~ 10% in total material lowers typical temperatures by less than 2°.

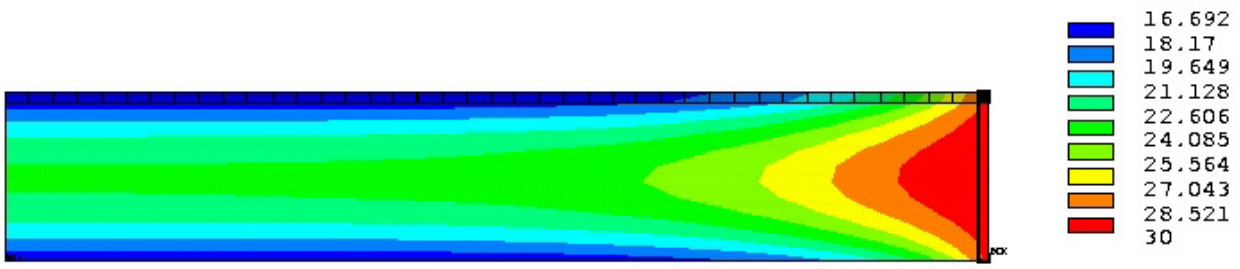
Table 2. ANSYS calculations for "optimized" configuration (°C).

location	scheme C	"optimized"
Tension plate	30	29
ASDBLR (PCB)	30	29
ASDBLR (chip surface)	30	30
DTMROC (PCB)	42	33
DTMROC (chip surface)	60	46
Upper cooling plate	19	19

Effect of tension plate temperature on module temperature

Because the overall module temperature uniformity, and thus, gas gain, can be affected if the tension plate gets too hot, we generated an ANSYS model to study this situation. The important boundary elements for this case are the cooling tube running the length of the module, which is the only means for removal of module heat, and the two heat sources, namely the electronics heat from the ends and the overall module heating from the particle flux in the detector. Since the same fluid cools the module and the electronics in series, it is important to determine which should be cooled first, i.e. with the colder fluid. Fig. 6 shows the output for these two cases. In both runs the tension plate temperature was fixed at 30° and the type 1 module (non-electronic) heat load was 274 W / m³, corresponding to 7.4 W over the whole module, applied where radiator is present. In case (a) the cooling tube is fixed at 14°, and in case (b) at 20°, representing sending the coolant through the electronics first. Due to symmetry, the model only needs to represent a half-length module, so the horizontal scale in these figures is 0.75 meter, with the tension plate on the right. The lengthwise cut shown here does not pass through either of the cooling tubes at the corners, so the lowest visible temperatures are higher than 14° and 20°, respectively. The figures show that the temperature uniformity within the module is improved (a ΔT of 11° vs. 14°) by using the higher cooling fluid temperature, with only a 1° increase at the tension plate. This supports the proposal that cooling fluid should be routed first through the electronics and then through the module.

(a) $T_{cooling}$ = 14°



(b) $T_{cooling}$ = 20°

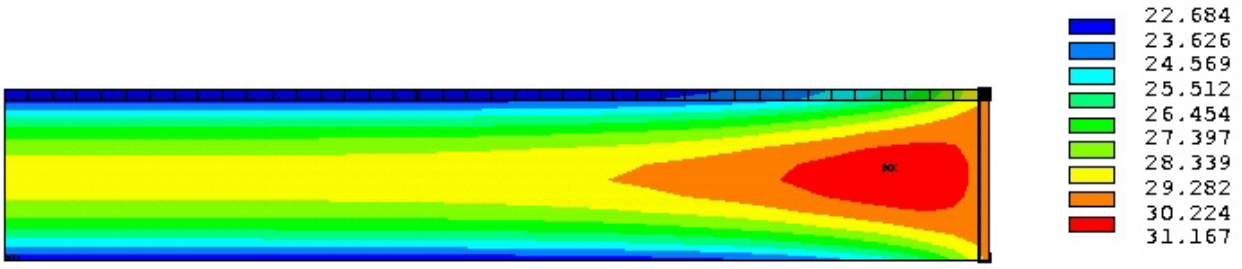


Fig. 6. ANSYS output of module cooling FEA calculations.

Conclusions

The main conclusion from these studies is that scheme C provides adequate cooling for the electronics and minimizes the tension plate temperature. Some specific recommendations for the design of the flex circuit are that the insulation below the DTMROC be present and the upper stamp board have as good an out-of-plane thermal conductivity as possible. Additionally, the cooling fluid should be sent through the electronics before the module.